

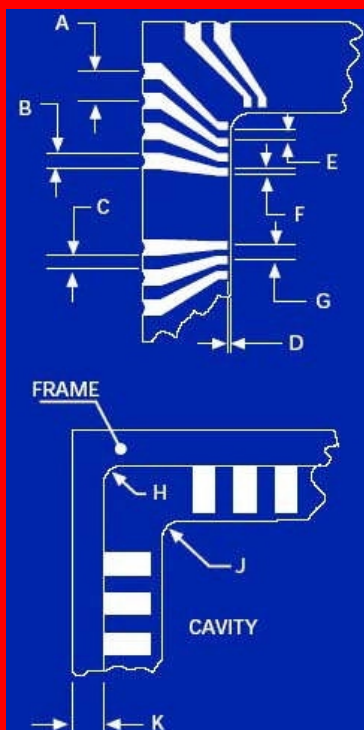
Highly reliable leadless Chip Carriers that are manufactured from Polymer materials.

## BENEFITS & OPTIONS:

- More economical
- Lower weight
- Matches PCB Thermal characteristics
- Sturdy construction
- Fully customizable interconnect
- Customer specific or JEDEC footprint
- Multilayer metallization available
- Supplied as single units or arrays for large area assembly
- Solder mask options available

## USAGE:

- Die attach using conductive or non-conductive adhesive
- Gold thermosonic or Aluminium ultrasonic wire bondable finish available
- Chip protection with Epoxy, Silicone Gel or 'B' stage epoxy lid
- Lid seal with pre-screened B stage epoxy, oven cured
- Surface mount - solder attach using IR or vapour phase reflow



## SPECIFICATIONS

Base Material	BT	HTBE
Foil Thickness	18µm	18µm
Colour	Brown (Natural)	Black
TG	185°C	160°C
TCE	13-18 ppm/°C	13-16 ppm/°C
Volume Resistivity	3x10 <sup>14</sup> ohms	3x10 <sup>14</sup> ohms
Dielectric Constant	3.9	4.2
Mechanical / Dimension Tolerance		
Outside dimensions	±0.05 mm max	±0.05 mm max
Cavity	±0.075 mm max)	±0.075 mm max
Flatness	±0.06 mm/cm max	±0.06 mm/cm max
Plating		
Copper	1.4µm (nominal)	1.4µm (nominal)
Nickel	10µm (nominal)	10µm (nominal)
Gold	0.5µm (nominal)	0.5µm (nominal)
Electrical Performance (based on APEC 40-40 AC)		
Leakage lead to lead	< 0.5nA at 400v	< 0.5nA at 400v
Lead resistance	< 0.1 ohm	< 0.1 ohm
Lead inductance	< 5nH	< 5nH
Capacitance lead to lead	0.2pF	0.2pF
Temperature Limits		
Storage Temperature	-65°C - +150°C	-65°C - +150°C
Operating Temperature	-40°C - +150°C	-40°C - +150°C
Typical vertical Thermal Properties (based on Apec 40-40 AC)		
Standard Thermal Resistance	92°C/W	92°C/W
Low TH design (vias not soldered)	30°C/W	30°C/W
Low TH design (vias soldered)	10°C/W	10°C/W

## GENERAL DESIGN RULES

Dimension	Description	
A	Pitch at castellation	0.50 mm min
B	Line width at castellation	0.30 mm min
C	Line to line clearance at castellation	0.20 mm min
D	Die pad/cavity to bond finger tip	0.25 mm min
E	Line to line clearance at bond site	0.10 mm min
F	Line width at bond site	0.10 mm min
G	Pitch at bond site	0.20 mm min
H	Radius at frame corner	0.40 mm min
J	Corner radius 2 and 3 level versions	0.40 mm min
K	Frame width	0.38 mm min

Hole diameter	0.25 mm min with 5:1 aspect ratio
Land diam (outer layers)	0.45 mm min
Land diam (inner layers)	0.6 mm min
Solder mask annular ring	0.3 mm (screened) 0.15 mm (photo-imaged)
Position tolerance	±0.3 mm (screened) ±0.10 mm (photo-imaged)



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